In The Specification

Please replace paragraph starting at page 2, line 8 with the following:

In a data read operation, if a column address signal CAS and a write command WR are at a high level, a read command signal CSLR is applied to the transistor TR1 at a high level, and thus the Sense AMP 150 is activated, and the transistor TR1 is turned ON (meaning active, conducting current). At least one of the Sense Amp transistors ~~TR3~~ TR2 or TR3 detects the minute voltage signal on its respective bit line (BL or BLB) and "amplifies" it. Then, data in the bit line pair (BL and BLB) is output to first and second output lines (RIO and RIOB). In a data read operation, a write signal CSLW becomes low, and thus the transistors TR4 and TR5 are turned OFF.